High efficiency DC-DC Buck converter architecture suitable for embedded applications using switched capacitor

Patitapabana Pani, Dr. B.V.V.Subhramanya Kumar

School of Electronics, KIIT University, Bhubaneswar, Odisha, India

ABSTRACT: *Here we look inside how the switched capacitor has evolved over the passage of years with special emphasis to the dc-dc buck converter. It also discusses why there is a strong potential to further the study related to designs based around a switched capacitor Buck Converter for embedded applications. The main objective of the paper is to look into the controller design for minimizing size, enhancing efficiency and reliability of power converters in portable electronic equipment such as mobile phones and PDAs. The converter is designed in 0.18- m CMOS process to get regulated 1.3–1.6 V output from 3.3 V input supply. The buck converter is designed by using simple block called as cross coupled converter.*

Keywords— switched capacitors, buck converter, dual sc converter, cross-coupled converter, shoot through current, NRTI converter.

I.   INTRODUCTION

Over the years as the portable electronics industry progressed, different requirements evolved such as increased battery lifetime, small and cheap systems, brighter, full colour displays and demand for increased talk time in cellular phones.To keep up with these demands engineers have worked towards developing efficient conversion techniques and also has resulted in the subsequent formal growth of an interdisciplinary field of Power Electronics. Long back switched capacitors are used for DC-DC converters. But now-a-days it's the trend to use these SC based DC-DC converter for embedded power management applications in order to achieve high power efficiency and power density. In spite of the popularity of switched-capacitor dc-dc converters, the amount of literature devoted to their understanding and analysis is surprisingly small. Thus, the objective of this work is to present a modelling technique believed to be applicable to practical switched-capacitor dc-dc converter topologies. The technique leads naturally to a quantitative description of converter performance and to useful dc sign criteria. There are three types of switched capacitors which have given emphasis in this paper, they are dual sc converter, and cross coupled dual sc converter and NRTI converter. Here we propose a low voltage low ripple dual switch capacitor based hybrid DC-DC converter which is suitable for high dropout embedded regulation. In the proposed topology, along with a linear regulator two switching capacitors are used to store and recycle the charge for better power efficiency. The linear regulator is used to reduce the amount of output voltage ripple that comes from the switching capacitors. NRTI based cross-coupled buck converter avoids design complexity and synchronization of control signal. Here we propose to monitor the load current and change the switching frequency continuously to maintain power efficiency high. This flatness of the efficiency becomes possible due to the absence of shoot through current in the converter.
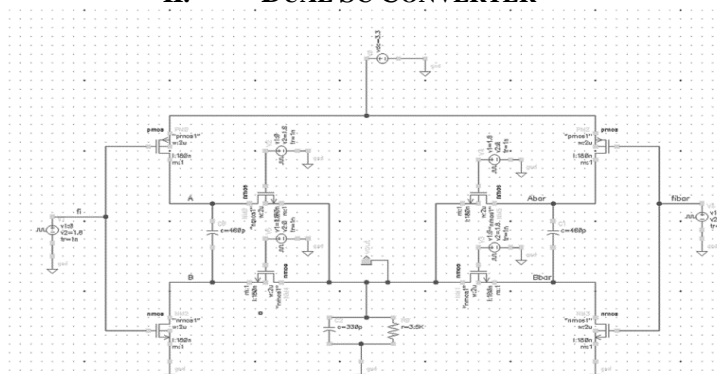
II.   DUAL SC CONVERTER

Fig.1. Screen shot diagram of dual SC converter

Basic schematic diagram of dual sc dc-dc buck converter is shown in fig 1.

In the circuit eight MOS switches are used including two PMOS and six NMOS switches. Two flying capacitors C_{f1} and C_{f2} are connected in the circuit having equal value. In phase Φ the capacitor C_{f2} operates between V_{dd} and V_{out} and this mode of operation is known as charging mode, during this time the other capacitor C_{f1} is connected between V_{out} and ground and this mode of operation is known as charge recycling mode. In phase Φ capacitor C_{f2} is connected between V_{out} and ground i.e. in charge recycling mode and the other capacitor C_{f1} is connected between Vdd and Vout (charging mode).
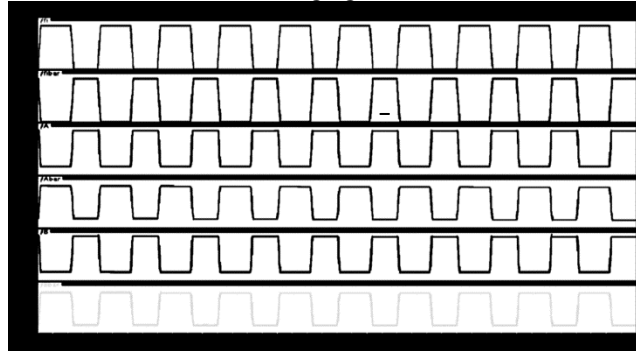

Fig.2. screen shot timing diagram of dual sc converter using cadence tool
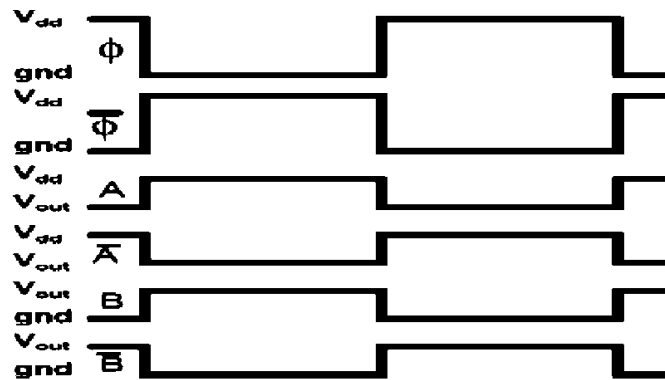

Fig.3 detailed view of signals at internal points of dual sc converter

Ignoring the resistance of the switches in steady state the average output voltage is $V_{dd}/2$. Here it is to be noted that all the transistors used should have gate-source and gate-drain tolerance limit at least V_{dd}. In the charging phase of flying capacitor C_{f1} voltage at node A is V_{dd} and in charge recycling phase voltage at same node A is V_{out}. Similarly voltage at node B during charging phase is V_{out} and in charge recycling phase is 0V. The vice versa happens during the case of C_{f2}.
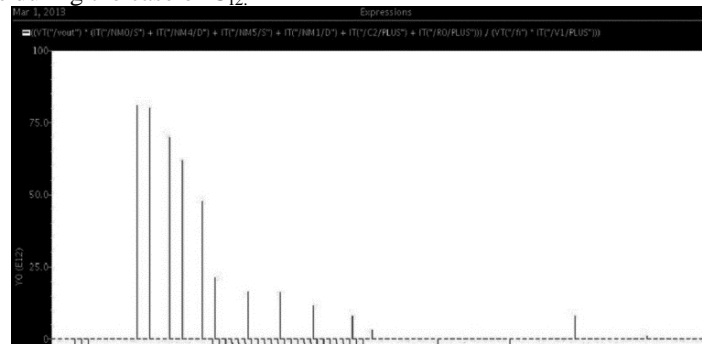

Fig.4. efficiency curve of dual sc converter showing 83%   power efficiency

The above fig shows the efficiency of dual sc converter. When an SC converter operates away from its unloaded conversion ratio, its efficiency suffers. Its maximum possible power efficiency, can be calculated by

$$Eff = \frac{output\ power}{input\ power}$$

III. CROSS COUPLED DUAL SC CONVERTER

From the waveform in fig.2 and fig.3 it is clear that the phases of voltages at node A and B are the same as those of the controlling signal Φ. similarly on the other hand phase of voltage at node A and B are same as of the signal Φ. But the signal swings at the internal nodes of the converter is generally half that of external control signal. With this observation in mind we introduce a converter shown in below figure which is referred to as cross-coupled dual sc converter.
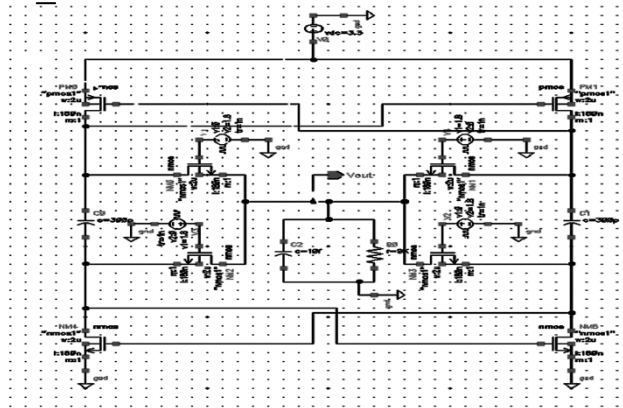

Fig.5 screen shot of cross-coupled dual sc converter

In cross-coupled dual sc converter the swing of signal is applied at the gate of four switches are reduced by a factor of half, then the corresponding switching loss of those switches reduce by a factor of one fourth. Here we can note that loss of drive strength of the four switches due to their gate – source voltage reduction may be compensated by replacing dual oxide transistor with the generally used normal transistor.

The loss is low in this circuit because there are no diode-wired MOSFETs and their associated threshold voltage problems. The circuit also has the advantage that the ripple frequency is doubled because there are effectively two voltage doublers both supplying the output from out of phase clocks.

But similar to normal dual sc converter, the cross coupled converter also suffers and faces short circuit power loss problem.

Fig.6 timing diagram of cross-coupled dual sc converter.

IV. NRTI CONVERTER

To overcome the short circuit power loss we use NRTI converter which is the proposed converter. The NRTI switching scheme can result in elimination of short in normal converter. Here switching scheme with 3-element based NRTI cross coupled converter is illustrated and then in my future work it will be extended to higher number of elements for better results in efficiency and density. By introducing more elements we can reduce the short circuit switching loss and so we can enhance the efficiency of the resulting converter.

The figure 7 shows the circuit diagram of a 3-element cross coupled converter. In the circuit there are 24 MOS switches and 6 flying capacitors are being used.
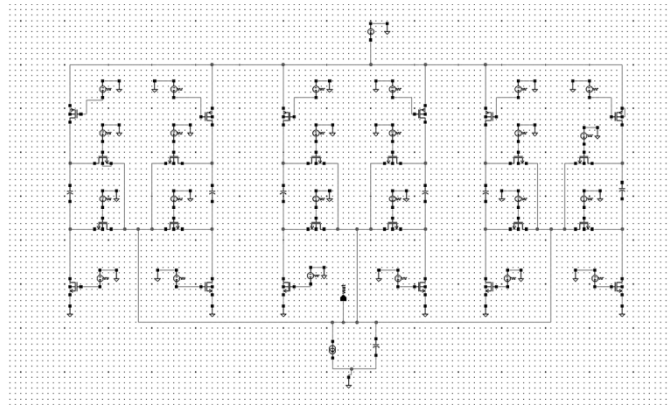
Fig.7 diagram of 3-element cross-coupled NRTI converter.

NRTI based cross-coupled converter also uses low signal swing to control half of its switches hence switching loss for the converter is decreased. At the same time half of the switches are driven by internal control signals, power loss to generate the control signal is almost reduced to half. In addition the internal control voltage have low swing which helps to use thin oxide transistor making switch smaller and reducing the power further.
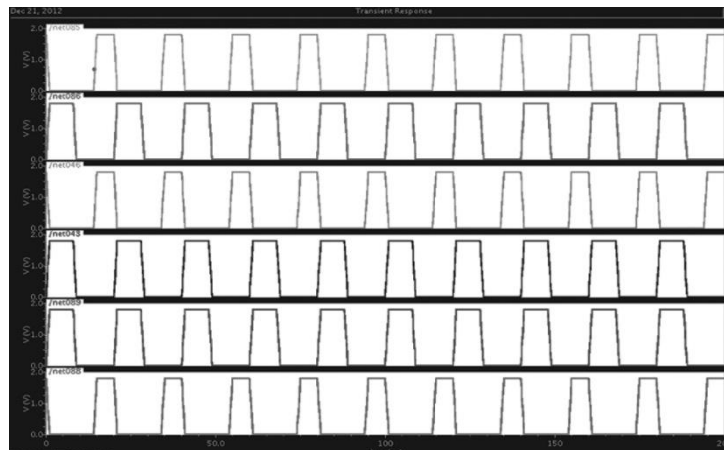

Fig. 8 timing diagram of NRTI converter.

3-element cross-coupled converter can be extended for higher number of elements to reduce capacitive overhead and output ripple at the cost of control circuit complexity and reduction of non- overlapping time. As number of element is increased there is a marginal increment of power efficiency. A careful analysis of power losses have been done to get high power efficiency over a wide range of load current while output ripple is maintained low. In absence of shoot through power loss in the converter, main source of power losses are switching and conduction power loss. switching power loss is directly proportional to square of control signal swing and width of transistor, while conduction power is inversely proportional to the overdrive voltage of MOSFET and width of the transistor. Total power loss in the converter can be minimized by maintaining conduction power loss and switching power loss equal.

V.   RESULTS
At first dual sc converter is designed in 0.18- m CMOS process with output of 1.35 volt. The power efficiency is improved up to 83% which is better than previous simulated results. Then to enhance the efficiency more cross coupled converter is designed. Then 3-element NRTI converter is designed for better power efficiency and elimination of short in the previous converters.

VI.   CONCLUSION
Power efficiency of the proposed converter is improved by reducing switching loss of the converter. Power efficiency is further improved and output ripple is reduced by eliminating shoot through current during switching transition.

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